INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD

Abstract of the Disclosure

Structures and methods for DEAPROM memory with low tunnel barrier intergate insulators are provided. The DEAPROM memory includes a first source/drain region and a second source/drain region separated by a channel region in a substrate. A floating gate opposes the channel region and is separated therefrom by a gate oxide. A control gate opposes the floating gate. The control gate is separated from the floating gate by a low tunnel barrier intergate insulator having a tunnel barrier of less than 1.5 eV. The low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of NiO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, Y_2O_3, Gd_2O_3, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$. The floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator. And, the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.